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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10038870	01/08/2002	716	5	2825	Dinh

* APPLICANTS: Johannsen Peer;

CONTINUING DATA VERIFIED:

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** FOREIGN APPLICATIONS VERIFIED:

GERMANY 10100433.8 01/03/2001

EUROPEAN PATENT OFFICE (EPO) 01108653.5 04/05/2001

PG-PUB DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		
Verified and Acknowledged Examiners's initials		1454.1210

TITLE : Method of circuit verification in digital design

U.S. DEPT. OF COMM. / PAT & TM-PTO-435L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs. Drwg.
		Print Fig.	
Primary Examiner		Application Examiner	
PREPARED FOR ISSUE			
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ISSUE FEE

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